

APPLICATION  
FOR  
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TITLE: METHOD AND APPARATUS FOR REDUCING SUB-  
THRESHOLD OFF CURRENT FOR A REAL TIME CLOCK  
CIRCUIT DURING BATTERY OPERATION

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METHOD AND APPARATUS FOR REDUCING SUB-THRESHOLD OFF CURRENT  
FOR A REAL TIME CLOCK CIRCUIT DURING BATTERY OPERATION

**PRIOR APPLICATION**

This application is a continuation of U.S. Patent serial no. 09/469,986, filed December 21, 1999.

**BACKGROUND**

5       The present application teaches a circuit for use in reducing power consumption of a real time clock in a computer system.

When a personal computer is turned off, an on-board battery, e.g. a 3-volt lithium battery, may still power certain  
10       circuits in the computer. For example, a real time clock often still maintains the time using battery power when the primary computer power supply goes offline.

The smaller transistors that are now used to make such circuits in order to fit more transistors on a substrate, often  
15       have higher leakage currents. These transistors consume undesired current when they are biased to the "off" state. This increases the DC load that is placed on the battery, when the computer power supply is off due to off state current, which can cause the battery to deplete more quickly.

20       **SUMMARY**

The present disclosure defines a device which reduces power consumption during battery powered operation of the Real Time Clock.

25       The application discloses a leakage reduction device for a real time clock system, that has a real time clock circuit, having separated first and second power supply connections, and maintaining a count indicative of real time; and an associated

circuit, which operates in a first mode when a power supply voltage is present and operates in a second mode when battery power is present, said second mode providing a biasing condition that minimizes off state leakage current during battery operation.

### DESCRIPTION OF DRAWINGS

These and other aspects will be described in detail with reference to the accompanying drawings, wherein:

Figure 1 shows a schematic diagram of the circuitry including the real time clock well.

Figure 2 shows a block diagram of a power monitoring embodiment.

### DETAILED DESCRIPTION

The present application describes reducing the undesired current flow through transistors in a clock circuit. In an embodiment, the transistors are MOS devices. The sub-threshold off current of these MOS devices is reduced by applying a voltage bias to the substrate relative to the gate, source and drain voltages. The relative device threshold voltage is then increased according to the relation

$$\Delta V_t = \left[ \frac{(2\epsilon_0 \epsilon_{ox} q N_a)^{1/2}}{C_{ox}} \right] \cdot \left[ (2\phi_f - V_{bias})^{1/2} - (2\phi_f)^{1/2} \right]$$

The sub-threshold off current is also reduced according to the relation

$$I_{off} = I_o \cdot e^{\frac{q}{KT} ((V_{gs} - (V + \Delta V_t)) \ln)} \left( 1 - e^{\frac{q}{KT} V_{DS}} \right)$$

with

$$I_o = \frac{\mu_v C_{ox} W_{eff}}{L_{eff}} \cdot \left( \frac{KT}{q} \right)^2 e^{1.8}$$

A schematic diagram of a specific circuit, e.g., a computer chipset, is shown in Figure 1. This circuit includes a real time clock circuit portion 100 that has separate power supply connections for the battery and for the wired power supply. The part that is always powered is separated from other circuits in the chip. The real time clock 100 is called the "RTC well" since it has the separate power supply connections. The separated connection enables battery 110, e.g., a 3.0 volt lithium battery, to be used to power the real time clock well while the remainder of the circuit is turned off.

An off-chip diode network has been used to isolate the battery from the computer's power supply once the computer is actually turned on.

The present application discloses circuitry forming a relative substrate bias which reduces the off current ( $I_{off}$ ) of the real time clock circuit during battery operation. This is done by changing source voltage levels in the real time clock well when the main power supply is turned off.

Switching devices, described in more detail herein, are connected between the source and substrate connections of N-channel and P-channel real time clock devices in the well 100. This better isolates the substrate from the N-channel source connection and isolates the N well from the P-channel source connection during battery operation. These switches are in one state when primary chip power or "core power" is available. The switches are in another state when the primary chip power is off and the real time clock circuit 100 is powered by the battery 110. In this latter state, the bias voltage of the real time clock is raised to a level that decreases leakage. The real

time clock logic continues to operate at the raised source voltage condition during the low-leakage battery operation.

The circuit and its control are illustrated in Figure 1. The RTC well 100 has three power connection nodes. The  $V_{n\_source}$  power node 112 of the real time clock module 100 is controlled  
 5 by N-channel switching transistor ( $N_s$ ) 116. Energizing  $N_s$  116 selectively switches the  $V_{n\_source}$  node 112 to the  $V_{ss}$  ground rail. When transistor 116 is deenergized, node 112 floats.

P-channel device well nodes of the real time clock include  
 10  $V_{p\_sub}$  120, and  $V_{p\_source}$  122. Multiplexers 124 and 132 control the power supplied to these nodes. These multiplexers can be thick-gate P-channel MOS devices. The  $V_{p\_sub}$  node is controlled by multiplexer 124. One input 126 to the multiplexer 124 is the core 1.3 volt power line 130 from power supply 131. The other  
 15 input 128 to the multiplexer 124 is a power consumption-reducing bias level  $N_{bias1}$ . This bias level is formed by the biasing resistors 140, 142, 144 placed across the battery 110.

Analogously, the multiplexer 132 receives the core power supply 1.3 volts 130 at its one input, and a second bias level  
 20  $N_{bias2}$  at the other input thereof.

These bias levels are selected to minimize the leakage.  $V_{p\_sub}$  (120) can be 2.0 volts, and  $V_{p\_source}$  (122) can be 1.6 volts.

Level shifting logic, including  $N_{VD1}$  (152),  $N_{VD2}$  (148),  $P_{TG1}$  (154), and  $P_{TG2}$  (156) control the switching of the multiplexers  
 25 124 and 132. When core power 130 is present, inverter 146 is enabled and controls the gate voltages of the n-channel devices  $N_s$  116 and  $N_{VD2}$  148.

In normal operation, when the power supply 131 is on, an output voltage is produced on line 130. The inserter 146 is  
 30 enabled, producing a high output that pulls up the gate voltage of the devices  $N_s$  116 and  $N_{VD2}$  148. Biasing  $N_{VD2}$  148 turns on  $N_s$  116 and connects the N-channel source node  $V_{n\_source}$  to ground 114.

Biasing of  $N_{VD1}$  152 causes  $P_{TG1}$  and  $P_{TG2}$  to raise the multiplex control line 125, switching the multiplexer units 124, 132. This connects the nodes  $V_{p_{sub}}$  and  $V_{p_{source}}$  to the core 1.3 volt power 130.

5        When core power 130 is not available, the real time clock 100 operates under battery power. The output of  $V_{TG3}$  158 pulls up the input to the inverter 146, thereby lowering the output of the inverter 146, and turning off the gate of  $N_{VD2}$  148 and  $N_s$  116.  $N_s$  116 isolates  $V_{n_{source}}$  from ground 114. The multiplexer units  
10       124, 132 are also caused to switch, thereby connecting the real time clock nodes  $V_{p_{sub}}$  120 and  $V_{p_{source}}$  122 to the bias voltages  $N_{bias1}$  and  $N_{bias2}$ , respectively. This also causes device  $P_{TG4}$  162 to turn on, to establish the bias levels  $bias_1$  and  $bias_2$  across the resistor ladder, 140, 142, 144 using battery power. The bias  
15       resistors should be larger than 10 M ohms, to minimize current flow from the battery.

This circuit even further conserves battery power since the bias resistors are isolated from the battery during non-battery operation.

20       As noted above, these bias values are selected as values that will allow the RTC logic and oscillator circuits in the well 100 to operate at low leakage current levels. Selected bias levels include  $V_{n_{source}}$  at 0.4 volts,  $V_{p_{sub}}$  at 2.0 volts and  $V_{p_{source}}$  at 1.6 volts.

25       The circuits in the real time clock well should continue to operate at all times. Capacitors  $C1$ ,  $C2$ ,  $C3$  are used to decouple any switching noise during the transition between the two modes of operation to prevent the registers from being corrupted during a transition between the normal operation and  
30       the low leakage battery-powered operation.

These capacitors have a value of, for example 10pF. In summary, the on and off conditions of the circuits during the two modes of operation are listed below in Table 1.

5

TABLE 1

<u>1.3V Core Power ON:</u> <u>(normal operation)</u>		<u>1.3V Core Power OFF:</u> <u>(low leakage operation)</u>	
$N_S$	ON		OFF
$N_{VD1}$	OFF		ON
$N_{VD2}$	ON		OFF
$P_{TG1}$	ON		OFF
$P_{TG2}$	OFF		ON
$P_{TG3}$	ON		OFF
$P_{TG4}$	OFF		ON
$N_{bias1}$	OFF		ON
$N_{bias2}$	OFF		ON
$V_{nsource}$	0V		0.4V
$V_{nsub}$	0V		0V
$V_{psource}$	1.3V		1.6V
$V_{psub}$	1.3V		2.0V

A second embodiment is shown in block diagram form in Figure 2. A hardware monitor device 200 monitors characteristics of the computer, including temperature, power supply level and other information. The device 200 produces a "power okay signal" when the power supply is up and running. This "power okay" signal is delayed by delay element 202 (e.g., a capacitor), and then drives the gates of  $N_{VD2}$  and  $N_S$  instead of the inverter 146 shown in the first embodiment.

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Use of the power okay signal may help to isolate the real time clock well 100 from rail noise during a turn on sequence. For example, the hardware monitor could use a delay mechanism as

shown, e.g., the power okay signal would only be produced after the power supply is stabilized. This keeps the real time well 100 isolated until the power supply is sufficiently stable.

Although not described in detail herein, other embodiments  
5 fall within the spirit and scope of the disclosed invention, as set forth in the appended claims.